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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,410	04/20/2005	Chiu-Hao Cheng	USP2958T-ZTCL	8123

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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/531,410	CHENG ET AL.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because the abstract contains the numbers of the elements located within the drawings. These numbers need to be deleted from the specification. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Brown et al. (USPN 6360340B1). As per claim 1, Brown et al. discloses a control circuit adapted for reading a test data from said test sample in column 2, lines 61-65; a memory, having a predetermined memory space, controlled by said control circuit to store said test data in column 3, lines 9-12; a compressor electrically coupled between said control circuit and said memory to compress said test data for reducing a size thereof before storing in said memory, such that said compressed test data is stored in said memory space of said memory to maximize said memory space of said memory to be utilized for storing a complete series of said test data of said test sample in column 3, lines 4-12; and a transmission interface electrically connected to said control circuit for

communicating connecting to a computer having a display means, wherein when said memory space of said memory is used up, said control circuit fetches said test data in said memory for directly transmitting said fetched test data to said computer through said transmission interface so as to display said fetched test data on said display means in column 5, lines 19-27.

4. As per claim 2, Brown et al. discloses wherein said control circuit controls said compressor for decompressing said fetched test data before transmitting said fetched test data to said computer in column 3, lines 6-12.

5. As per claim 3, Brown et al. discloses wherein said control circuit reads a test data in digital form from said test sample which embodies as a digital circuit in column 2, lines 46-53. The pattern generator generates data in digital form.

6. As per claim 4, Brown et al. discloses wherein said control circuit reads a test data in digital form from said test sample which embodies as a digital circuit in column 2, lines 46-53. The pattern generator generates data in digital form.

7. As per claim 5, Brown et al. discloses wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time internal in column 2, lines 50-51.

8. As per claim 6, Brown et al. discloses wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time internal in column 2, lines 50-51.

9. As per claim 7, Brown et al. discloses a control circuit adapted for reading a test data from said test sample in column 2, lines 61-65; a memory, having a predetermined

memory space, controlled by said control circuit to store said test data in column 3, lines 9-12; a compressor electrically coupled between said control circuit and said memory to compress said test data for reducing a size thereof before storing in said memory, such that said compressed test data is stored in said memory space of said memory to maximize said memory space of said memory to be utilized for storing a complete series of said test data of said test sample in column 3, lines 4-12; and a display means electrically coupling with said compressor, wherein when said memory space of said memory is used up, said control circuit fetches said test data in said memory to display said fetched test data on said display panel in column 5, lines 19-27.

10. As per claim 8, Brown et al. discloses wherein said control circuit controls said compressor for decompressing said fetched test data before displaying said fetched test data on said display means in column 3, lines 6-12.

11. As per claim 9, Brown et al. discloses wherein said control circuit reads a test data in digital form from said test sample which embodies as a digital circuit in column 2, lines 46-53. The pattern generator generates data in digital form.

12. As per claim 10, Brown et al. discloses wherein said control circuit reads a test data in digital form from said test sample which embodies as a digital circuit in column 2, lines 46-53. The pattern generator generates data in digital form.

13. As per claim 11, Brown et al. discloses wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time internal in column 2, lines 50-51.

14. As per claim 12, Brown et al. discloses wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time internal in column 2, lines 50-51.

15. As per claim 13, Brown et al. discloses a control circuit, a memory, and a compressor, comprising the steps of: (a) reading said test data from said test sample to said control circuit in column 2, lines 61-65; (b) compressing said test data by said compressor to reduce a size of said test data in column 3, lines 4-12; (c) storing said compressed test data in said memory to maximize a memory space of said memory to be utilized for storing a complete series of said test data of said test sample in column 3, lines 9-12; and (d) displaying said test data on a display means which is electrically coupled with said compressor, wherein when said memory space of said memory is used up, said control circuit fetches said test data in said memory to display said fetched test data on said display panel in column 5, lines 19-27.

16. As per claim 14, Brown et al. discloses wherein said control circuit is electrically connected to a computer via a transmission interface to transmit said fetches said test data to said computer so as to display said fetches said test data on said display means built-in with said computer when said memory space of said memory is used up in column 5, lines 19-27.

17. As per claim 15, Brown et al. discloses after the step (c), further comprising a step of decompressing said fetched test data before displaying said fetched test data on said display panel in column 3, lines 6-12.

18. As per claim 16, Brown et al. discloses after the step (c), further comprising a step of decompressing said fetched test data before displaying said fetched test data on said display panel in column 3, lines 6-12.

19. As per claim 17, Brown et al. discloses in step (a), wherein said control circuit reads a test data in digital form from said test sample which embodies as a digital circuit in column 2, lines 46-53. The pattern generator generates data in digital form.

20. As per claim 18, Brown et al. discloses in step (a), wherein said control circuit reads a test data in digital form from said test sample which embodies as a digital circuit in column 2, lines 46-53. The pattern generator generates data in digital form.

21. As per claim 19, Brown et al. discloses wherein said control circuit reads a test data in digital form from said test sample which embodies as a digital circuit in column 2, lines 46-53. The pattern generator generates data in digital form.

22. As per claim 20, Brown et al. discloses in step (a), wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time internal in column 2, lines 50-51.

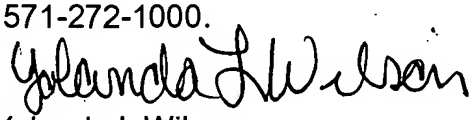
23. As per claim 21, Brown et al. discloses in step (a), wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time internal in column 2, lines 50-51.

24. As per claim 22, Brown et al. discloses in step (a), wherein said control circuit reads said test data including high/low potential status of every pin of said test sample at a fixed time internal in column 2, lines 50-51.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Yolanda L Wilson
Examiner
Art Unit 2113